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# 328612(28)

## B. E. (Sixth Semester) Examination, April-May 2021

**(Old Scheme)**

**(Et&T Engg. Branch)**

## ADVANCED ELECTRONIC CIRCUITS

***Time Allowed : Three hours***

***Maximum Marks : 80***

***Minimum Pass Marks : 28***

***Note :*** *Attempt all questions. Part (a) is compulsory from each question. Attempt any* ***two*** *parts from (b), (c) and (d).*

### Unit-I

**1.** (a) What is the advantage of inverted R – 2R DAC over R – 2R DAC ladder network? 2

(b) Draw and explain the circuit of dual slope Analog to Digital converter in detail. 7

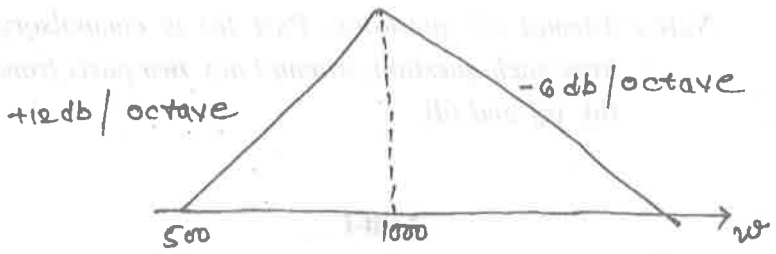
(c) Draw & explain the diagram of Delta Modulation type Analog to Digital converter. 7

(d) A 10 bit Digital to Analog converter has a step size of 10 mV. Determine the full scale output voltage and its percentage resolution. 7

## Unit-II

2. (a) Explain the meaning of bilinear Transfer function. 2

(b) Design a filter for the plot given below and determine half power frequency. 7








(c) Write down different steps for designing of inverting opamp and non inverting op-amp. How can we analyse the necessity of the filter? 7

(d) What is the need to add fourth opamp in biquad circuit & also derive the expression of four opamp biquad circuit with frequency response. 7

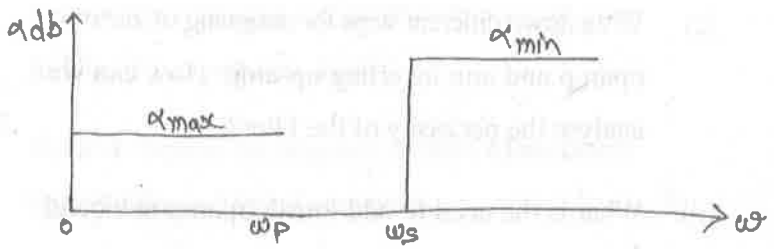
## Unit-III

3. (a) Explain RC – CR transformation. 2

(b) Design a low pass Butterworth Response from the given specifications $\alpha_{max} = 0 \cdot 5$ db, $\alpha_{min} = 30$ db, $K = A_0 = 1$, $w_p = 750$ rad/sec, $w_s = 1750$ rad/sec, use scaling in the final design. 7

(c) Explain with circuit diagram the working of Deylliannis-Friend's circuit. 7

(d) The following specifications are given for a Chebyshev low pass filter : $w_p = 1$ rad/sec, $w_s = 2 \cdot 33$ rad/sec, $\alpha_{max} = 0 \cdot 5$ db and $\alpha_{min} = 22$ db design a filter. 7




## Unit-IV

4. (a) Define Lock Range and Capture Range. 2

(b) A PLL has a VCO with $K_0 = 25$ kHz/V and $f_c = 50$ kHz. The amplifier gain is $A = 2$ and the phase detector has a maximum output voltage swing of ±0·7 V. Find the lock range of PLL. Assume filter gain to unity. 7

(c) Explain the operation of IC 565 VCO and explain its operation. 7

(d) Derive the expression for lock range & capture range of phase locked loop. 7

## Unit-V

5. (a) What is the mean of Quadrant of multiplier? 2





(b) Draw & explain the working of logrithmic multiplier. 7

(c) Write the application of multiplier circuit & explain multiplier as phase detector. 7

(d) Explain how to get square root and square of the given analog signal? 7